Electrical Yield and Reliability Issues of Ultra High Density Interposers and Update on Advanced Integration Program at BRIDG

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Abstract

The continuing advance of Internet based activity, including mobile devices, connected sensors and cloud based operations, is driving the microelectronics industry to come up with faster devices and smaller form factors. The traditional route to CMOS miniaturization via device level scaling is reaching its limit. Our advanced integration program is aimed at developing solutions which address this challenge through innovative technologies aimed at package level scaling on a conventional silicon platform.

The Ultra High Density Interposer project is focused on developing stacked interposers with signal input/output (I/O) an order of magnitude higher than typically achieved. There are several pre and post processing challenges associated with such interposer development. This presentation will provide an analysis on the electrical yield and reliability issues of ultra high density interposers. A status overview of the advanced integration program being pursued at BRIDG will also be provided.